Curriculum Vitæ

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Biography

Sarma Vrudhula is a Professor in the School of Computing, Informatics and Decisions Systems Engineering at Arizona State University, Tempe AZ. He received the B.Math (Honors) from the University of Waterloo, Ontario, Canada, in 1976 and his M.S. and Ph.D degrees in electrical engineering from the University of Southern California in 1980 and 1985, respectively. During 1985-1992 he was on the faculty of the EE-Systems department of the University of Southern California. From 1992 to 2005 he was a professor in the Electrical and Computer Engineering department at the University of Arizona, in Tucson, AZ.

In 1996 he established the NSF Center for Low Power Electronics (CLPE) at the University of Arizona, in collaboration with the EE department of the Arizona State University. CLPE was supported by the NSF, the State of Arizona, and many leading companies in the microelectronics industry. Through CLPE, he has facilitated the research of twenty faculty and over 40 graduate students across both campuses. He is also the founding director of the NSF I/UCRC Center for Embedded Systems at ASU.

His work spans several areas in design automation and computer aided design for digital integrated circuit and systems, focusing on energy management of circuits and systems. Specific topics include: energy optimization of battery powered computing systems and wireless sensor networks; system level dynamic power and thermal management of multicore processors and system-on-chip (SoC); statistical methods for the analysis of process variations; statistical optimization of performance, power and leakage; new circuit architectures of threshold logic circuits for the design of ASICs and FPGAs; technology mapping with threshold logic circuits; the implementation of threshold logic using spintronic devices, and non-Boolean computation in emerging technologies. His teaching experience includes both undergraduate and graduate courses in digital systems design and testing, VLSI design, CAD algorithms for VLSI, advanced synthesis and verification methods, computer architecture, and discrete mathematics.

He has served on the technical program committees of many national and international conferences in VLSI design automation and CAD, and on government review panels. He served as an Associate Editor for the IEEE Transactions on VLSI, and is presently an Associate Editor for the IEEE Transaction on CAD, and the ACM Transactions on Design Automation of Electronic Systems (TODAES). During the 2000-2001, he was a visiting scientist with the Advanced Design Tools group in Motorola, Austin.

He was made Fellow of the IEEE in 2016 for "*contributions to low power and energy-efficient design of digital circuits and systems.*"

Education

B.Math Mathematics and Computer Science, 1976
University of Waterloo, Waterloo, Canada.

M.S. Electrical Engineering, 1981
University of Southern California, Los Angeles.

Ph.D. Electrical Engineering, 1985
University of Southern California, Los Angeles.

Employment

Feb. '09 - Present	Director, NSF IUCRC Consortium for Embedded Systems
Jan. '05 - Present	Professor, Computer Science and Engineering Dept., Arizona State University, Tempe AZ.
Apr. '96 - Dec. '04	Director, NSF S/IUCRC Center for Low Power Electronics University of Arizona, Tucson, AZ.
Apr. '96 - Dec. '04	Professor, Electrical and Computer Engineering Dept. University of Arizona, Tucson, AZ
Aug. '92 - July '96	Associate Professor, Electrical and Computer Engineering Dept. University of Arizona, Tucson, AZ
Jan. '85 - Aug. '92	Assistant Professor, Dept. of Electrical Enginering-Systems University of Southern California, Los Angeles, CA.
Sept. '81 - Dec. '84	Research Assistant, Dept. of Electrical Enginering-Systems University of Southern California, Los Angeles, CA.
Apr. '82 - Sept. '82	Member of Technical Staff, IBM, Hopewell Junction, NY.
June '78 - Sept. '81	Member of Research Staff, USC Information Sciences Institute Marina Del Rey, CA.
Sept. '76 - Sept. '77	Member of Technical Staff, Bell Canada, Toronto, Canada.

Journals

[72] N. Kulkarni, J. Yang, J.-S. Seo, and S. Vrudhula, "Reducing Power, Leakage and Area of Standard Cell ASICs Using Threshold Logic Flipflops," *IEEE Transactions on VLSI*, vol. 24, pp. 2873–2886, Sept. 2016.

[71] A. Winther, W. Liu, A. Nannarelli, and S. Vrudhula, "Thermal aware floorplanning incorporating temperature dependent wire delay estimation," *Microprocessors and Microsystems (MICPRO), Elsevier*, no. 39, pp. 807–815, 2015.

[70] L. Gao, I.-T. Wang, P.-Y. Chen, S. Vrudhula, J.-S. Seo, Y. Cao, T.-H. Hou, and S. Yu, "Fully parallel write/read in resistive synaptic array for accelerating on-chip learning," *Nanotechnology*, vol. 26, pp. 1–9, Nov. 2015.

[69] J.-S. Seo, B. Lin, M. Kim, P.-Y. Chen, D. Kadetotad, Z. Xu, A. Mohanty, S. Vrudhula, S. Yu, J. Ye, and Y. Cao, "On-chip sparse learning acceleration with cmos and resistive synaptic devices," *IEEE Transactions on Nanotechnology*, vol. 14, pp. 969–979, Nov. 2015.

[68] D. Mahalanabis, V. Bharadwaj, H. J. Barnaby, S. Vrudhula, and M. N. Kozicki, "A non-volatile sense amplifier flip-flop using programmable metallization cells," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 5, pp. 205–213, June 2015.

[67] D. Kadetotad, Z. Xu, A. Mohanty, P.-Y. Chen, B. Lin, J. Ye, S. Vrudhula, S. Yu, Y. Cao, and J.-S. Seo, "Parallel architecture with resistive crosspoint array for dictionary learning acceleration," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS*, vol. 5, pp. 194–204, June 2015.

[66] Z. Xu, P. An, Y. Cao, M. Cavaliere, and S. Vrudhula, "The Stochastic Loss of Spikes in Spiking Neural P Systems: Design and Implementation of Reliable Arithmetic Circuits," *ACM Fundamenta Informaticae*, vol. 134, pp. 183–200, Jan. 2014.

[65] D. Mahalanabis, Y. Gonzalez-Velo, H. Barnaby, M. N. Kozicki, P. Dandamudi, and S. Vrudhula, "Impedance Measurement and Characterization of Ag-Ge30Se70 based Programmable Metallization Cells," *IEEE Transactions on Electron Devices*, vol. 61, pp. 3723–3730, Nov. 2014.

[64] D. Mahalanabis, H. J. Barnaby, Y. Gonzalez-Velo, M. N. Kozicki, S. Vrudhula, and P. Dandamudi, "Incremental Resistance Programming of Programmable Metallization Cells for Use as Electronic Synapse," *Solid State Electronics*, vol. 100, pp. 39–44, Oct. 2014.

[63] V. Hanumaiah, D. Desai, B. Gaudette, C.-J. Wu, and S. Vrudhula, "STEAM: A Smart Temperature and Energy Aware Multicore Controller," *ACM Transactions on Embedded Computing Systems*, vol. 13, Sept. 2014.

[62] S. N. Nukala, N. Kulkarni, and S. Vrudhula, "Spintronic Threhsold Logic Array (STLA) - A Compact, Low Power, Non-Volatile Gate Array Architecture," *Journal of Parallel and Distributed Computing*, vol. 74, pp. 2452–2460, June 2014.

[61] V. Hanumaiah and S. Vrudhula, "Energy-efficient Operation of Multi-core Processors by DVFS, Task Migration and Active Cooling," *IEEE Transactions on Computers*, vol. 63, pp. 349–360, Feb. 2014.

[60] B. Gaudette, V. Hanumaiah, S. Vrudhula, and M. Krunz, "Maximizing Quality of Coverage under Connectivity Constraints in Solar Powered Active Wireless Sensor Networks," *ACM Transactions on Sensor Networks*, vol. 10, Nov. 2013.

[59] V. Hanumaiah and S. Vrudhula, "Temperature-aware DVFS for Hard Real-Time Applications on Multi-core Processors," *IEEE Transactions on Computers*, vol. 61, Oct. 2012.

[58] V. Hanumaiah, S. Vrudhula, and K. Chatha, "Performance Optimal Online DVFS and Task Migration Techniques for Thermally Constrained Multi-core Processors," *IEEE Transactions on Computer-Aided Design (TCAD)*, vol. 30, pp. 1677–1690, Nov. 2011.

[57] T. Gowda, S. Vrudhula, N. Kulkarni, and K. Berezowski, "Identification of Threshold Functions and Synthesis of Threshold Networks," *IEEE Transactions on Computer-Aided Design (TCAD)*, vol. 30, pp. 665–677, May 2011.

[56] A. Shrivastava, D. Kanan, S. Bhardwaj, and S. Vrudhula, "Reducing Functional Unit Power Consumption and its Variation using Leakage Sensors," *IEEE Transactions on Very Large Scale Integration (VLSI)*, vol. 18, pp. 988–997, Jul. 2010.

[55] W. Wang, S. Yang, S. Bhardwaj, S. Vrudhula, F. Liu, and Y. Cao, "The Impact of NBTI Effect on Combinational Circuits: Modeling, Simulation and Analysis," *IEEE Transactions on Very Large Scale Integration (VLSI)*, vol. 18, pp. 173–183, Feb. 2010.

[54] R. Rao and S. Vrudhula, "Fast and Accurate Prediction of the Steady State Throughput of Multi-Core Processors Under Thermal Constraints," *IEEE Transactions on Computer-Aided Design (TCAD)*, vol. 28, pp. 1559–1572, Oct. 2009.

[53] A. Goel, S. Vrudhula, F. Taraporevala, and P. Ghanta, "Statistical timing models for large macro cells and IP blocks considering process variations," *IEEE Transactions on Semiconductor Manufacturing*, vol. 22, no. 1, pp. 3–11, 2009.

[52] T. Gowda, S. Vrudhula, and S. Kim, "Prediction of pair-wise gene interaction using threshold logic," *Annals of New York Academy of Sciences (NYAS)*, vol. 1158, no. 1, pp. 276–286, 2009.

[51] T. Gowda, S. Vrudhula, and S. Kim, "Modeling of gene regulatory network dynamics using threshold logic," *Annals of New York Academy of Sciences (NYAS)*, vol. 1158, no. 1, pp. 71–81, 2009.

[50] J. Zhuo, C. Chakrabarti, K. Lee, N. Chang, and S. Vrudhula, "Maximizing the lifetime of embedded systems powered by fuel cell-battery hybrids," *IEEE Transactions on Very Large Scale Integration (VLSI)*, vol. 17, no. 1, pp. 22–32, 2009.

[49] K. Lee, B. Gwon, J. Kim, N. Chang, S. Kadri, S. Vrudhula, J. Zhuo, and C. Chakrabarti, "Design and evaluation of fuel-cell battery hybrid power source for human portbale embedded systems," *ACM Transactions on Design Automation of Electronic Systems*, vol. 13, no. 1, pp. 19:1–19:34, 2008.

[48] S. Bhardwaj and S. Vrudhula, "Leakage minimization of digital circuits using gate sizing in the presence of process variations," *IEEE Transactions on Computer Aided Design*, vol. 27, pp. 445–455, March 2008.

[47] S. Bhardwaj, S. Vrudhula, and A. Goel, "A unified approach to full chip statistical timing and leakage analysis of nanoscale circuits considering intra-die variations," *IEEE Transactions on Computer-Aided Design*, vol. 27, no. 10, pp. 1812–1825, 2008.

[46] S. Bhardwaj and S. Vrudhula, "Multiattribute optimization with application to leakage delay trade-offs using utility theory," *Journal of Low Power Electronics (JOLPE)*, vol. 4, pp. 68–80, 2008.

[45] S. Bhardwaj, W. Wang, R. Vattikonda, K. Cao, and S. Vrudhula, "A scable model for predicting the effect of nbti for reliable design," *IET Circuits, Devices and Systems*, vol. 2, pp. 361–371, Aug. 2008.

[44] K. Berezowski and S. Vrudhula, "Multiple-valued logic circuits design using negative differential resistance devices," *Journal of Multiple-Valued Logic and Soft Computing*, vol. 13, no. 4-6, pp. 447–466, 2007.

[43] R. Rao and S. Vrudhula, "Energy optimal speed control of a produce-consumer device pair," *ACM Transactions on Embedded Computing Systems*, vol. 6, no. 4, pp. 30/1–30/30, 2007.

[42] P. Ghanta and S. Vrudhula, "Analysis of power supply noise in the presence of process variations," *IEEE Design & Test of Computers*, vol. 24, pp. 256–266, June 2007.

[41] S. Bhardwaj, K. Cao, and S. Vrudhula, "Statistical leakage minimization of digital circuits using gate sizing, gate length biasing and threshold voltage minimization," *Journal of Low Power Electronics (JOLPE)*, vol. 2, no. 2, pp. 240–250, 2006.

[40] R. Rao and S. Vrudhula, "Energy optimal speed control of a generic device," *IEEE Transactions on Computer Aided Design*, vol. 25, no. 12, pp. 2737–2746, 2006.

[39] K. Chopra and S. Vrudhula, "Efficient symbolic algorithms for computing the minimum and bounded leakage states," *IEEE Transactions on Computer Aided Design*, vol. 25, no. 12, pp. 2820–2832, 2006.

[38] S. Vrudhula, J. Wang, and P. Ghanta, "Hermite polynomial based interconnect analysis in the presence of process variations," *IEEE Transactions on Computer Aided Design*, vol. 25, no. 10, pp. 2001–20011, 2006.

[37] T. Shu, M. Krunz, and S. Vrudhula, "Joint optimization of transmit power-time and bit energy efficiency in cdma wireless sensor networks," *IEEE Transactions on Wireless Communications*, vol. 5, no. 11, pp. 3109–3118, 2006.

[36] S. Dasika, S. Vrudhula, and K. Chopra, "Algorithms for optimizing lifetime of battery powered wireless sensor networks," *Sensor Network Operations, IEEE Press*, May 2006.

[35] S. Bhardwaj, S. Vrudhula, and D. Blaauw, "Probability distribution of signal arrival times using bayesian networks," *IEEE Transactions on Computer Aided Design*, vol. 24, pp. 1784–1794, November 2005.

[34] L. Znamirowski, O. Palusinski, and S. Vrudhula, "Programmable analog/digital arrays in control and simulation," *Kluwer Internaltional Journal on Analog Integrated Circuits and Signal Processing*, pp. 55–73, April 2004.

[33] D. Rakhmatov, S. Vrudhula, and D. Wallach, "A model for battery lifetime analysis for organizing applications on a pocket computer," *IEEE Transactions on VLSI Systems*, pp. 1019–1030, December 2003.

[32] R. Rao, S. Vrudhula, and D. Rakhmatov, "Battery modeling for energy-aware system design," *IEEE Computer, Special issue on Power-Aware & Temperature-Aware Computing*, vol. 36, pp. 77–87, December 2003.

[31] D. Rakhmatov and S. Vrudhula, "Energy management for battery-powered embedded systems," *ACM Transactions on Embedded Computing Systems*, vol. 2, pp. 277–324, August 2003.

[30] S. Vrudhula, D. Blaauw, and S. Sirichotiyakul, "Probabilistic analysis of interconnect coupling noise in deep submicron circuits," *IEEE Transactions on Computer Aided Design*, August 2003.

[29] H. Wang and S. Vrudhula, "Behavioral synthesis of field programmable analog array circuits," *ACM Transactions on Design Automation of Electronic Systems*, vol. 7, pp. 563–603, October 2002.

[28] Q. Wang and S. Vrudhula, "Algorithms for minimizing standby power in dual-v_th cmos circuits," *IEEE Transactions on Computer Aided Design*, vol. 21, pp. 2054–2116, March 2002.

[27] O. Palusinski, S. Vrudhula, L. Znamirowski, and D. Humbert, "Microreactor process control using field programmable analog array technology," *Journal of Chemical Engineering Progress*, vol. 97, pp. 60–66, August 2001.

[26] D. Rakhmatov, S. Vrudhula, T. Brown, and A. Nagarandal, "Adaptive multi-user on-line reconfigurable engine," *IEEE Design & Test of Computers*, vol. 17, pp. 53–67, March 2000.

[25] Q. Wang, S. Vrudhula, G. Yeap, and S. Ganguly, "Power reduction and power-delay tradeoffs using logic tranformations," *ACM Transactions on Design Automation of Electronic Systems*, vol. 4, pp. 97–121, January 1999.

[24] H.-Y. Xie and S. Vrudhula, "A method for estimating signal activities in logic circuits by local propagation of transition probabilities," *Integrated Computer-Aided Engineering*, vol. 5, no. 2, pp. 141–152, 1998.

[23] R. Mackey, J. Rodriguez, J. Carothers, and S. Vrudhula, "Asynchronous VLSI architecture for adaptive echo cancellation," *Electronic Letters*, 1996.

[22] Y.-T. Lai, S. Vrudhula, and M. Pedram, "Formal verification using edge-valued binary decision diagrams," *IEEE Transactions on Computers*, vol. 45, pp. 247–255, February 1996.

[21] A. Majumdar and S. Vrudhula, "Fault coverage and test length estimation for random pattern testing," *IEEE Transactions on Computers*, vol. 44, pp. 234–247, February 1995.

[20] K. Ho and S. Vrudhula, "Interval graph algorithms for two dimensional multiple folding of array based VLSI layouts," *IEEE Transactions on Computer Aided Design*, vol. 13, pp. 1–22, October 1994.

[19] A. Majumdar and S. Vrudhula, "Techniques for estimating test length under random test," *Journal of Electronic Testing: Theory and Applications*, pp. 285–297, May 1994.

[18] Y.-T. Lai, S. Vrudhula, and M. Pedram, "Evbdd-based algorithms for linear integer programming, spectral transformation and function decomposition," *IEEE Transactions on Computer Aided Design*, vol. 13, no. 8, pp. 959–975, 1994.

[17] A. Majumdar and S. Vrudhula, "Analysis signal probability in logic circuits using stochastic models," *IEEE Transactions on VLSI Systems*, vol. 1, no. 3, pp. 365–379, 1993.

[16] T.-Y. Wuu and S. Vrudhula, "A design of a fast and area efficient muller-c element," *IEEE Transactions on VLSI Systems*, vol. 1, pp. 215–219, June 1993.

[15] A. Majumdar and S. Sastry, "Probabilistic characterization of controllability in general homogeneous circuits," *Computer-Aided Design*, vol. 25, pp. 76–93, February 1993.

[14] S. Sastry and A. Majumdar, "Test-efficiency analysis of random self-test of sequential circuits," *IEEE Transactions on Computer Aided Design*, vol. 10, pp. 390–398, March 1991.

[13] S. Sastry and J. Pi, "Estimating the minimum of partitioning and floorplanning problems," *IEEE Transactions on Computer Aided Design*, vol. 10, no. 2, pp. 273–282, 1991.

[12] C. Ravikumar, S. Sastry, and L. Patnaik, "Parallel min-cut placement on reduced hardware simd architecture," *Journal of Computer Systems Science and Engineering*, vol. 6, no. 1, pp. 3–11, 1991.

[11] C. Ravikumar and S. Sastry, "A parallel approach to three layer channel routing," in *CAD Accelerators* (A. P. Ambler, P. Agrawal, and W. R. Moore, eds.), Elsevier Science, 1991.

[10] C. Ravikumar and S. Sastry, "Lara : A layout accelerator based on reduced array architecture," in *CAD Accelerators* (A. P. Ambler, P. Agrawal, and W. R. Moore, eds.), Elsevier Science, 1991.

[9] C. Ravikumar and S. Sastry, "Vyuha: A detailed router for multiple routing models," *INTEGRATION: The VLSI Journal*, no. 11, pp. 141–157, 1991.

[8] C. Ravikumar and S. Sastry, "Placement accelerators," in *Progress in Computer Aided VLSI Design* (G. W. Zobrist, ed.), vol. 5, Ablex Publishers, 1990.

[7] C. Ravikumar and S. Sastry, "Parallel placement on hypercube architecture," *Int'l Journal of Computer Aided VLSI Design*, vol. 2, pp. 159–179, 1990.

[6] C. Ravikumar and S. Sastry, "Hierarchical vlsi routing on a reduced hardware simd architecture," *Int'l Journal of Computer Aided VLSI Design*, vol. 2, pp. 45–63, 1990.

[5] C. Ravikumar and S. Sastry, "A hardware accelerator for hierarchical vlsi routing," *Integration: The VLSI Journal*, no. 7, pp. 283–302, 1989.

[4] C. Ravikumar, S. Sastry, and L. Patnaik, "Parallel circuit partitioning on a reduced array architecture," *Computer Aided Design*, vol. 21, no. 7, pp. 447–455, 1989.

[3] S. Sastry and M. Breuer, "Detectability of cmos stuck-open faults using random and pseudo random test sequences," *IEEE Transactions on Computer Aided Design*, vol. 7, no. 9, pp. 933–946, 1988.

[2] V. P. Kumar and S. Sastry, "Efficient signal processing on a vlsi array," *IEEE Transactions on Circuits and Systems*, vol. 35, no. 9, pp. 1103–1113, 1988.

[1] S. Sastry and A. Parker, "Stochastic models for wirability analysis of gate arrays," *IEEE Transactions on Computer Aided Design*, vol. 5, no. 1, pp. 52–65, 1986.

Conferences

[151] N. Kulkarni, A. Dengi, and S. Vrudhula, "A Clock Skewing Strategy to Reduce Power and Area of ASIC Circuits," in *Proc. IEEE/ACM Design Automation Conf. (DAC)*, (Austin, TX), June 2017.

[150] M. Ince, S. Ozev, and S. Vrudhula, "Statistical Library Characterization Using Arbitrary Polynomial Chaos," in *Proc. IEEE Latin American Symp. on Circuits and Systems (LASCAS)*, (Bariloche, Argentina), Feb. 2017.

[149] Y. Ma, Y. Cao, S. Vrudhula, and J. sun Seo, "Optimizing Loop Operation and Dataflow in FPGA Acceleration of Deep Convolutional Neural Networks," in *Proc. IEEE Int'l. Symp. on Field-Programmable Gate Arrays*, (Monterey, CA), Feb. 2017.

[148] Y. Ma, N. Suda, J. sun Seo, Y. Cao, and S. Vrudhula, "Scalable and Modularized RTL Compilation of Convolutional Neural Networks onto FPGA," in *Proc. IEEE Int'l. Conf. on Field Programmable Logic and Applications*, Aug. 2016.

[147] D. Mahalanabis, M. Sivaraj, W. Chen, S. Shah, H. Barnaby, M. Kozicki, J. B. Christen, and S. Vrudhula, "Demonstration Of Spike Timing Dependent Plasticity in CBRAM Devices With Silicon Neurons," in *Proc. IEEE Int'l. Symp. on Circuits and Systems (ISCAS)*, May. 2016.

[146] J. Davis, N. Kulkarni, J. Yang, A. Dengi, and S. Vrudhula, "Digital IP Protection Using Threshold Voltage Control," in *Proc. IEEE Symp. Quality Electronic Design (ISQED)*, Mar. 2016.

[145] N. Suda, V. Chandra, G. Dasika, A. Mohanty, Y. Ma, S. Vrudhula, J. sun Seo, and Y. Cao, "Throughput-optimized opencl-based fpga accelerator for large-scale convolutional neural networks," in *Proc. IEEE Int'l. Symp. on Field-Programmable Gate Arrays (FPGA)*, (Monteray, CA), Feb. 2016.

[144] B. Gaudette, C.-J. Wu, and S. Vrudhula, "Improving Smartphone/Mobile User Experience by Balancing Performance and Energy with Probabilistic QoS Guarantee," in *Proc. IEEE Symp. on High Performance Computer Architecture (HPCA)*, Mar. 2016.

[143] Y. Ma, M. Kim, A. Mohanty, Y. Cao, J.-S. Seo, and S. Vrudhula, "Energy-Efficient Reconstruction of Compressively Sensed Bioelectrical Signals with Stochastic Computing Circuits," in *Proc. Int'l. Conf. on Computer-Aided Design (ICCD)*, Nov. 2015.

[142] J. Yang, J. Davis, N. Kulkarni, J.-S. Seo, and S. Vrudhula, "Dynamic and Leakage Power Reduction of ASICs Using Configurable Threshold Logic Gates," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, (San Jose, CA), Sept. 2015.

[141] S. Vrudhula, N. Kulkarni, and J. Yang, "Design of Threshold Logic Gates using Emerging Devices," in *Proceedings IEEE International Symposium on Circuits and Systems*, (Lisbon, Portugal), May 2015.

[140] J. Yang, N. Kulkarni, and S. Vrudhula, "Fast and Robust Differential Flipflops and their Extension to Multi-input Threshold Gates," in *Proceedings IEEE International Symposium on Circuits and Systems*, (Lisbon, Portugal), pp. 822 – 825, May 2015.

[139] N. Kulkarni, J. Yang, and S. Vrudhula, "A fast, energy efficient, field programmable threshold-logic array," in *International Conference on Field Programmable Technology*, (Shanghai, China), pp. 300 – 305, Dec. 2014.

[138] Z. Xua, Mohantya, Abinash, C. Pai-Yu, B. Lin, J. Ye, S. Vrudhula, S. Yu, J.-S. Seoa, and Y. Cao, "Parallel Programming of Resistive Cross-point Array for Synaptic Plasticity," in *Proceedings of the Symposium on Biomorphic Circuits and Systems with Threshold Logic*, (Boston, MA), Oct. 2014.

[137] D. Kadetotad, Z. Xu, A. Mohanty, P.-Y. Chen, B. Lin, J. Ye, S. Y. Sarma Vrudhula, Y. Cao, and J.-S. Seo, "Neurophysics-inspired Parallel Architecture of Resistive Crosspoint Array for Dictionary Learning," in *Proceedings of the Biomedical Circuits and Systems Conference (BioCAS)*, (Lausanne, Switzerland), Oct. 2014.

[136] J. Yang, N. Kulkarni, S. Yu, and S. Vrudhula, "Integration of Threshold Logic Gate Circuit with RROM Devices for Low Power, and Robust Operation," in *Proceedings of the IEEE/ACM Intenational Symposium on Nanoscale Architectures*, (Paris, France), July 2014.

[135] M. Hamzeh, A. Shrivastava, and S. Vrudhula, "Branch-Aware Loop Mapping on CGRAs," in *Proceedings of the 51 Design Automation Conference (DAC)*, (San Francisco, CA), June 2014.

[134] V. Hanumaiah, D. Desai, and S. Vrudhula, "Design of Optimal Closed Loop Controller and OS Scheduler for Dynamic Energy Management in Heterogeneous Multicore Processors." IEEE/ACM Design Automation Conference, Designer Track Presentation & Poster, June 2013. Nominated for Design Track Best Presentation.

[133] M. Hamzeh, A. Shrivastava, and S. Vrudhula, "Enhancing compiler techniques for energy-efficient programmable accelerators," in *Proceedings of the 49 Design Automation Conference (DAC)*, (Austin, TX), June 2013.

[132] N. Kulkarni, N. S. Nukala, and S. Vrudhula, "Minimizing area and power of sequential cmos circuits using threshold decomposition," in *Proceedings of the IEEE International Conference on Computer Aided Design (ICCAD)*, (San Jose, CA), Nov 2012.

[131] N. S. Nukala, N. Kulkarni, and S. Vrudhula, "Spintronic threshold logic array - a compact, low leakage, non-volatile gate array architecture," in *Proceedings of the IEEE/ACM International Symposium on Nanoscale Architectures*, (Amsterdam, Netherlands), July 4-6 2012.

[130] M. Hamzeh, A. Shrivastava, and S. Vrudhula, "Epimap: Using epimorphism to map applications on cgras," in *Proceedings of the 49 Design Automation Conference (DAC)*, (San Diego, CA), June 2012.

[129] B. Gaudette, V. Hanumaiah, S. Vrudhula, and M. Krunz, "Optimal range assignment in active solar powered sensor networks," in *Proceedings of the 31st Annual IEEE International Conference on Computer Communications (INFOCOM)*, (Orlando, Florida), Jan. 2012.

[128] A. Winther, W. Liu, A. Nannarelli, and S. Vrudhula, "Temperature dependent wire delay estimation in floorplanning," in *Proceedings of the 29th IEEE NORCHIP Conferene*, pp. 1–4, Nov. 2011.

[127] A. Shrivastava, J. Pager, R. Jeyapaul, M. Hamzeh, and S. Vrudhula, "Enabling Multi-threading on CGRAs," in *Proceedings of the International Conference on Parallel Processing (ICPP)*, Sep. 2011.

[126] G. Chalivendra, V. Hanumaiah, and S. Vrudhula, "A new balanced 4-moduli set $\{2^k, 2^n - 1, 2^n + 1, 2^{n+1} - 1\}$ and its reverse converter design for efficient FIR filter implementation," in *Proceedings of the GLSVLSI Symposium*, (Lausanne, Switzerland), May. 2011.

[125] N. Kulkarni and S. Vrudhula, "Technology mapping for power using threshold logic cells," in *Proceedings of the GLSVLSI Symposium*, (Lausanne, Switzerland), May. 2011.

[124] V. Hanumaiah and S. Vrudhula, "Reliability-aware thermal management for many-core processors," in *Proceedings of the Design, Automation & Test in Europe Conference (DATE)*, (Grenoble, France), Mar. 14-18 2011.

[123] S. Leshner, K. Berezowski, and S. Vrudhula, "Design of a robust, high performance standard cell threshold logic family for deep sub-micron technology," in *Proceedings of the IEEE International Conference on Microelectronics*, (Cairo, Egypt), Dec. 19-22 2010.

[122] S. Leshner, K. Berezowski, X. Yao, G. Chalivendra, S. Patel, and S. Vrudhula, "A low power, high performance threshold logic-based standard cell multiplier in 65 nm cmos," in *Proceedings of the IEEE Computer Society Annual Symposium on VLSI*, (Lixouri Kefalonia, Greece), July 5-7, 2010 2010.

[121] M. A. Baker, P. Dalale, K. S. Chatha, and S. Vrudhula, "A scalable parallel h.264 decoder on the cell broadband engine architecture," in *Proceedings of International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Oct. 11-16 2009.

[120] V. Hanumaiah, S. Vrudhula, and K. Chatha, "Maximizing performance of thermally constrained multi-core processors by dynamic voltage and frequency control," in *Proceedings of the IEEE International Conference on Computer Aided Design (ICCAD)*, (San Jose, CA.), Nov 2009.

[119] V. Hanumaiah, R. Rao, S. Vrudhula, and K. Chatha, "Throughput optimal task allocation under thermal constraints for multi-core processors," in *Proceedings of the IEEE/ACM Design Automation Conference (DAC)*, (San Francisco, CA.), July 2009.

[118] V. Hanumaiah, S. Vrudhula, and K. Chatha, "Performance optimal speed control of multi-core processors under thermal constraints," in *Proceedings of the Design, Automation & Test in Europe (DATE)*, (Nice, France), 20-24 March 2009.

[117] R. Rao and S. Vrudhula, "Efcient online computation of core speeds to maximize the throughput of thermally constrained multi-core processors," in *Proceedings of the IEEE International Conference on Computer Aided Design (ICCAD)*, (San Jose, CA), pp. 537–542, Nov. 2008.

[116] R. Rao, S. Vrudhula, and K. Berezowski, "Analytical results for design space exploration of multi-core processors employing thread migration," in *Proceedings of the ACM International Symposium on Low Power Electronics and Design (ISLPED)*, (Bangalore, India), pp. 229–232, 2008.

[115] A. Goel and S. Vrudhula, "Current source based cell models for statistical timing and signal integrity analysis," in *Proceedings of the IEEE/ACM Design Automation Conference (DAC)*, (Anaheim, CA), June 2008.

[114] A. Goel, S. Vrudhula, F. Taraporevala, and P. Ghanta, "A methodology for characterization of large macro cells and IP blocks considering process variations," in *Proceedings of the International Symposium on Quality Electronic Design (ISQED)*, (San Jose, CA), 17-19 March 2008. (Best Paper Award).

[113] S. Ramamoorthy, H. Wang, and S. Vrudhula, "A low-power double-edge-triggered address pointer circuit for FIFO memory design," in *Proceedings of the International Symposium on Quality Electronic Design (ISQED)*, 2008.

[112] A. Goel and S. Vrudhula, "Current source based standard cell model for accurate signal integrity and timing analysis," in *Proceedings of the Design Automation and Test in Europe Conference (DATE)*, (Munich, Germany), 10-14 March 2008.

[111] T. Gowda, S. Leshner, S. Vrudhula, and S. Kim, "Threshold logic gene regulatory model: Prediction of dorsal-ventral patterning and hardware based simulation of drosophila," in *Proceedings of the International Conference on Biomedical Electronics and Devices*, (Funchal, Madeira, Portugal), 28 January 2008.

[110] T. Gowda and S. Vrudhula, "A decomposition based approach for synthesis of multi-level threshold logic circuits," in *Proceedings of the Asia and South Pacific Design Automation Conference*, (Seoul, Korea), 21 January 2008.

[109] D. Kannan, A. Shrivastava, S. Bhardwaj, and S. Vrudhula, "Power reduction of functional units considering temperature and process variations," in *International Conference on VLSI Deisgn*, (Hyderabad, India), 4 January 2008.

[108] D. Kannan, A. Shrivastava, S. Bhardwaj, and S. Vrudhula, "Temperature and process variations aware power gating of functional units," in *International Conference on VLSI Deisgn*, (Hyderabad, India), 4 January 2008.

[107] T. Gowda, S. Leshner, S. Vrudhula, and G. Konjevod, "Synthesis of threshold logic using tree matching," in *Proceedings of the European Conference on Circuit Theory and Design (ECCTD)*, (Sevilla, Spain), 26 August 2007.

[106] R. Rao and S. Vrudhula, "Performance optimal processor throttling under thermal constraints," in *Proceedings of the ACM/IEEE International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, (Salzburg, Austria), pp. 257–266, 1-3 October 2007.

[105] R. Rao, S. Vrudhula, and C. Chakrabarti, "Throughput of multi-core processors under thermal constraints," in *Proceedings of the IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, (Portland, Oregon), 27-29 August 2007.

[104] A. Goel, S. Bhardwaj, P. Ghanta, and S. Vrudhula, "Computation of joint timing yield for sequential networks considering process variations," in *Proceedings of the International Workshop on Power, Timing, Modeling, Optimization and Simulation (PATMOS)*, (Goteborg, Sweden), 3-5 September 2007.

[103] T. Gowda, S. Leshner, S. Vrudhula, and S. Kim, "Threshold logic gene regulatory networks," in *Proceedings of the IEEE International Workshop on Genomic Signal Processing and Statistics (GENSIPS)*, (Tuusula, Finland), 10 June 2007.

[102] W. Wang, S. Yang, S. Bhardwaj, R. Vattikonda, S. Vrudhula, F. Liu, and Y. Cao, "The impact of NBTI on the performance of combinational and sequential circuits," in *Proceedings of the IEEE Design Automation Conference (DAC)*, (San Diego), pp. 364–369, 4 June 2007.

[101] T. Gowda, S. Vrudhula, and G. Konjevod, "A non-ILP based threshold logic synthesis methodology," in *Proceedings of the International Worshop on Logic Synthesis (IWLS)*, (San Diego), 30 May - 1 June 2007.

[100] K. Berezowski and S. Vrudhula, "Multiple-valued logic circuits using negative differential devices," in *Proceedings of the International Symposium on Multiple-Valued Logic*, (Oslo, Norway), 13 May 2007.

[99] T. Gowda, S. Vrudhula, and G. Konjevod, "Combinational equivalence checking for threshold circuits," in *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, (Stresa-Lago maggiore, Italy), 11 March 2007.

[98] S. Bhardwaj, P. Ghanta, and S. Vrudhula, "A fast and accurate approach for full chip leakage analysis of nano-scale circuits considering intra-die correlations," in *International Conference on VLSI Deisgn*, (Bangalore, India), January 2007.

[97] S. Bhardwaj, P. Ghanta, and S. Vrudhula, "A framework for statistical timing analysis using non-linear delay and slew models," in *Proceedings of the IEEE International Conference on Computer Aided Design (ICCAD)*, (San Jose, CA), November 2006.

[96] S. Bhardwaj, W. Wang, R. Vattikonda, K. Cao, and S. Vrudhula, "Predictive modeling of the NBTI effect for reliable design," in *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC)*, (San Jose, CA), 2006.

[95] R. Rao, S. Vrudhula, C. Chakrabarti, and N. Chang, "An optimal analytical solution for processor speed control with thermal constraints," in *Proceedings of the IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, (Tegernsee, Germany), pp. 292–297, 4-6 October 2006.

[94] J. Zhuo, C. Chakrabarti, N. Chang, and S. Vrudhula, "Maximizing the lifetime of embedded systems powered by fuel cell-battery hybrids," in *Proceedings of the IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, (Tegernsee, Germany), October 2006.

[93] J. Zhuo, C. Chakrabarti, N. Chang, and S. Vrudhula, "Extending the lifetime of fuel cell based hybrid systems," in *Proceedings of the IEEE Design Automation Conference (DAC)*, (San Francisco), July 2006.

[92] S. Bhardwaj, S. Vrudhula, P. Ghanta, and K. Cao, "Modeling of intra-die process variations for accurate analysis and optimization of nano-scale circuits," in *Proceedings of the IEEE Design Automation Conference (DAC)*, (San Francisco, CA), July 2006.

[91] P. Ghanta, S. Vrudhula, S. Bhardwaj, and R. Panda, "Stochastic variational analysis of large power grids considering intra-die correlations," in *Proceedings of the IEEE Design Automation Conference (DAC)*, (San Francisco, CA), July 2006.

[90] Y. Cho, N. Chang, S. Vrudhula, and C. Chakrabarti, "High-level power management of embedded systems with application specific energy cost functions," in *Proceedings of the IEEE Design Automation Conference (DAC)*, (San Francisco, CA), July 2006.

[89] P. Ghanta and S. Vrudhula, "Variational interconnect delay metrics for statistical timing analysis," in *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, (San Jose CA), March 2006.

[88] S. Bhardwaj, S. Vrudhula, and Y. Cao, "Lotus: Leakage optimization under timing uncertainty for standard-cell designs," in *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, (San Jose CA), March 2006.

[87] S. Bhardwaj, Y. Cao, and S. Vrudhula, "Statistical leakage minimization through joint selection of gate sizes, gate lengths and threshold voltage," in *Proceedings of the Asia and South Pacific Design Automation Conference*, (Yokohama City, Japan), January 2006.

[86] K. Berezowski and S. Vrudhula, "Automatic design of binary multiple-valued logic gates on the rtd series," in *Proceedings of the Eight Euromicro Conference on Digital System Design*, (Porto, Portugal), August 2005.

[85] S. Bhardwaj and S. Vrudhula, "Formalizing designer's preferences for multiattribute optimization with applications to leakage-delay tradeoffs," in *Proceedings of the IEEE International Conference on Computer Aided Design (ICCAD)*, pp. 713–718, November 2005.

[84] R. Rao, S. Vrudhula, and N. Chang, "Battery optimization vs energy optimization: Which to choose and when?," in *Proceedings of the IEEE International Conference on Computer Aided Design (ICCAD)*, (San Jose, CA), pp. 439–445, 6-10 November 2005.

[83] R. Rao and S. Vrudhula, "Energy optimal speed control of devices with discrete speed sets," in *Proceedings of the IEEE Design Automation Conference (DAC)*, (Anaheim, California), pp. 901–904, 13-17 June 2005.

[82] S. Bhardwaj and S. Vrudhula, "Leakage minimization of nanoscale circuits in the presence of systemaic and random variations," in *Proceedings of the IEEE Design Automation Conference (DAC)*, pp. 541–546, June 2005.

[81] T. Shu, M. Krunz, and S. Vrudhula, "Power balanced coverage time optimization for clustered wireless sensor networks," in *Proceedings of the ACM International Symposium on Mobile Ad Hoc Networking and Computing*, May 2005.

[80] P. Ghanta, S. Vrudhula, R. Panda, and J. Wang, "Stochastic power grid analysis considering process variations," in *Proceedings of the Design Automation and Test in Europe Conference (DATE)*, pp. 964–969, 2005.

[79] P. Ghanta, S. Bhardwaj, and S. Vrudhula, "Variational analysis of interconnects and power grids considering process variations," in *Proceedings of the ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, pp. 14–19, 2005.

[78] R. Rao and S. Vrudhula, "Disk drive energy optimization for audio-visual applications," in *Proceedings of the ACM/IEEE International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pp. 93–103, 22-25 September 2004.

[77] J. Wang, P. Ghanta, and S. Vrudhula, "Stochastic analysis of interconnect performance in the presence of process variations," in *Proceedings of the IEEE International Conference on Computer Aided Design (ICCAD)*, pp. 880–886, November 2004.

[76] R. Rao and S. Vrudhula, "Energy optimization for a two device dataflow chain," in *Proceedings of the IEEE International Conference on Computer Aided Design (ICCAD)*, (San Jose, California), pp. 268–274, 7-11 November 2004.

[75] K. Agarwal, D. Sylvester, D. Blaauw, F. Liu, S. Vrudhula, and S. Nassif, "Variational delay metrics for interconnect timing analysis," in *Proceedings of the IEEE Design Automation Conference (DAC)*, pp. 381–388, 2004.

[74] S. Raj, S. Vrudhula, and J. Wang, "A methodology for improving timing yield in the presence of process variations," in *Proceedings of the IEEE Design Automation Conference (DAC)*, pp. 448–453, 2004.

[73] K. Chopra and S. Vrudhula, "Implicit pseudo boolean enumeration algorithms for input vector control," in *Proceedings of the IEEE Design Automation Conference (DAC)*, pp. 767–772, June 2004.

[72] S. Raj, S. Vrudhula, and J. Wang, "Statistical gate sizing to minimize timing yield loss," in *Proceedings of the ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, 2004.

[71] S. Dasika, S. Vrudhula, and K. Chopra, "A framework for battery aware sensor management," in *Proceedings of the Design Automation and Test in Europe Conference (DATE)*, (Paris, France), pp. 962–967, February 2004.

[70] R. Sreeramaneni and S. Vrudhula, "Energy profiler for hardware/software codesign," in *International Conference on VLSI Deisgn*, pp. 335–340, 2004.

[69] K. Chopra, S. Vrudhula, and S. Bhardwaj, "Efficient algorithms for identifying the minimum leakage states in CMOS combinational logic," in *International Conference on VLSI Deisgn*, pp. 240–245, January 2004.

[68] S. Bhardwaj, S. Vrudhula, and D. Blaauw, "**TAU** : Timing analysis under uncertainity," in *Proceedings of the IEEE International Conference on Computer Aided Design (ICCAD)*, pp. 615–620, November 2003.

[67] R. Rao, S. Vrudhula, and D. Rakhmatov, "Analysis of discharge techniques for multiple battery systems," in *Proceedings of the IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, (Seoul, Korea), pp. 44–47, August 2003.

[66] A. Agarwal, D. Blaauw, V. Zolotov, and S. Vrudhula, "Computation and refinement of statistical bounds on circuit delay," in *Proceedings of the IEEE Design Automation Conference (DAC)*, pp. 348–353, June 2003.

[65] A. Agarwal, D. Blaauw, V. Zolotov, and S. Vrudhula, "Statistical timing analysis using bounds," in *Proceedings of the Design Automation and Test in Europe Conference (DATE)*, pp. 62–67, March 2003.

[64] A. Agarwal, D. Blaauw, V. Zolotov, and S. Vrudhula, "Statistical timing analysis using bounds and selective enumeration," in *Proceedings of the ACM/IEEE International Workshop*

on Timing Issues in the Specification and Synthesis of Digital Systems, pp. 25–31, December 2002.

[63] S. Bhardwaj, S. Vrudhula, and D. Blaauw, "Estimation of signal arrival times in the presence of delay noise," in *Proceedings of the IEEE International Conference on Computer Aided Design (ICCAD)*, pp. 418–422, November 2002.

[62] G. Zareba, O. Palusinski, S. Vrudhula, D. Allee, and W. Mensch, "Analysis, implementation and testing of an analog-to-digital over-sampling converter in a field programmable analog array," in *Proceedings of the International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES)*, (Warsaw, Poland), June 2002.

[61] D. Rakhmatov, S. Vrudhula, and D. Wallach, "Battery lifetime prediction for energy-aware computing," in *Proceedings of the IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 154–159, August 2002.

[60] D. Rakhmatov and S. Vrudhula, "Hardware-software bipartitioning for dynamically reconfigurable systems," in *Proceedings of the International Symposium on Hardware/Software Codesign*, 6 May 2002.

[59] S. Vrudhula, D. Blaauw, and S. Sirichotiyakul, "Estimation of the likelihood of capacitive coupling noise," in *Proceedings of the IEEE Design Automation Conference (DAC)*, pp. 653–658, June 2002.

[58] D. Rakhmatov, S. Vrudhula, and C. Chakrabarti, "Battery-conscious task sequencing for portable devices including voltage/clock scaling," in *Proceedings of the IEEE Design Automation Conference (DAC)*, June 2002. 189-194.

[57] D. Rakhmatov and S. Vrudhula, "A analytical high-level battery model for use in energy management of portable electronic systems," in *Proceedings of the IEEE International Conference on Computer Aided Design (ICCAD)*, pp. 488–493, November 2001.

[56] D. Rakhmatov and S. Vrudhula, "Minimizing routing configuration cost in dynamically reconfigurable fpgas," in *Proceedings of International Parallel and Distributed Processing Symp.*, pp. 23–27, April 2001.

[55] H. Wang, S. Vrudhula, and O. Palusinski, "Performance driven placememnt and routing for field programmable analog arrays," in *Proceedings of the International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES)*, (Zakopane, Poland), pp. 207–212, June 2001. (Outstanding Paper Award).

[54] G. Zareba, O. Palusinski, S. Warecki, and S. Vrudhula, "Data communication and control in mixed-signal development system," in *Proceedings of the International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES)*, (Zakopane, Poland), pp. 121–124, June 2001.

[53] D. Rakhmatov and S. Vrudhula, "Time-to-failure estimation for batteries in portable electronic systems," in *Proceedings of the IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, (Huntington Beach CA.), pp. 6–7, August 2001.

[52] H. Wang, S. Vrudhula, and O. Palusinski, "Behavioral level analog synthesis for field programmable analog arrays," in *Proceedings of the International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES)*, (Gdynia, Poland), pp. 91–95, June 2000.

[51] S. Warecki, O. Palusinski, S. Vrudhula, and W. Mensch, "Analog digital development board for rapid prototyping mixed signal circuits," in *Proceedings of the International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES)*, (Gdynia, Poland), pp. 85–90, June 2000.

[50] S. Vrudhula, "Power optimization techniques for logic circuits," in *Proc. Int'l. Conf. on Advances in Infrastructure for Electronic Business, Science, and Education on the Internet*, July 2000.

[49] Q. Wang and S. Vrudhula, "An investigation of power-delay tradeoffs for Dual V_T CMOS circuits," in *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, (Austin, Texas), pp. 556–562, October 1999.

[48] Q. Wang and S. Vrudhula, "A new short circuit power model for complex CMOS gates," in *Proceedings of IEEE Alessandro Volta Memorial Workshop on Low Power Design (Volta99)*, (Como Italy), pp. 98–106, March 1999.

[47] C. Reider, L. Znamirowski, O. Palusinski, S. Vrudhula, and D. Rakhmatov, "Dynamically reconfigurable analog/digital hardware implementation using fpga and fpaa technologies," in *Proceedings of International Conference on Simulation and Multimedia in Engineering Education*, January 1999.

[46] A. Pandey, V. Ramadurai, A. Mangudi, M. Gebreyesus, S. Vrudhula, and O. Palusinski, "Perforamance comparison of filters implemented in field programmable gate arrays and field programmable analog arrays," in *Proceedings of International Conference on Simulation and Multimedia in Engineering Education*, January 1999.

[45] Q. Wang and S. Vrudhula, "Static power optimization of deep submicron CMOS circuits for Dual V_T technology," in *Proceedings of the IEEE International Conference on Computer Aided Design (ICCAD)*, (San Jose, CA), pp. 153–159, November 1998.

[44] Q. Wang and S. Vrudhula, "Efficient procedures for minimizing the standby power in Dual V_T CMOS circuits," in *Proceedings of the International Workshop on Power, Timing, Modeling, Optimization and Simulation (PATMOS)*, (Technical University of Denmark, Lyngby, Denmark), pp. 19–28, October 1998.

[43] Q. Wang and S. Vrudhula, "On short circuit power estimation of CMOS inverters," in *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, (Austin, Texas), pp. 70–75, October 1998.

[42] Q. Wang and S. Vrudhula, "Data driven power optimization of sequential circuits," in *Proceedings of the Design Automation and Test in Europe Conference (DATE)*, (Paris, France), pp. 686–691, March 1998.

[41] H. Wang and S. Vrudhula, "A low-voltage, low-power ring pointer for use in a fifo memory," in *Proceedings of the SIUCRC Symp.*, (Norman Oklahoma), pp. 7–21 – 7–26, 1997.

[40] E. Tsun and S. Vrudhula, "Rapid prototyping of asynchronous multiple function unit network," in *Proceedings of the Rapid Systems Prototyping Conference*, (Chapel Hill, NC), pp. 63–69, June 1997.

[39] K. McCarley and S. Vrudhula, "Macro instruction generation for dynamic logic caching," in *Proceedings of the Rapid Systems Prototyping Conference*, (Chapel Hill, NC), pp. 157–166, June 1997.

[38] Q. Wang and S. Vrudhula, "Optimization of sequential circuits without global resets by structural transformations," in *Proceedings of the International Workshop on Logic Synthesis*, May 1997.

[37] Q. Wang, S. Vrudhula, and S. Ganguly, "An investigation of power delay trade-offs using logic and structural transformations:experiments on the powerpc," in *Proceedings of the IEEE Design Automation Conference (DAC)*, (Anaheim CA), pp. 425–428, June 1997.

[36] Q. Wang and S. Vrudhula, "Multi-level optimization for low power using local logic transformations," in *Proceedings of the IEEE International Conference on Computer Aided Design (ICCAD)*, (San Jose, CA), pp. 270–277, November 1996.

[35] S. Vrudhula, Y.-T. Lai, and M. Pedram, "Efficient computation of the probability and reed-muller spectra of boolean functions using edge-valued binary decision diagrams," in *Proceedings of the IFIP Workshop on Applications of Reed-Muller Expansion in Circuit Design*, (Makuhari, Chiba Japan), pp. 62–69, August 1995.

[34] R. Mackey, J. Rodriguez, J. Carothers, and S. Vrudhula, "A single-chip asynchronous echo canceller for high-speed data communications," in *Proceedings of the IEEE International ASIC Conference*, pp. 181–184, 1995.

[33] S. Vrudhula and H.-Y. Xie, "Techniques for CMOS power estimation and logic synthesis for low power," in *Proceedings of the International . Workshop on Low Power Design*, (Napa Valley, CA.), pp. 21–26, April 1994.

[32] Y.-T. Lai, M. Pedram, and S. Vrudhula, "FGLIP: An integer linear program solver based on function graphs," in *Proceedings of the IEEE International Conference on Computer Aided Design (ICCAD)*, pp. 685–689, November 1993.

[31] S. Vrudhula and A. Majumdar, "Models for estimating test length and fault coverage in random testing," in *Proceedings of the International Workshop on The Economics of Design, Test & Manufacturing for Electronic Circuits and Systems*, (Austin, Texas), pp. 8–13, May 1993.

[30] Y.-T. Lai, K. Pan, M. Pedram, and S. Vrudhula, "FGMap: A technology mapping algorithm for look-up table type fpgas based on function graphs," in *Proceedings of the International Worshop on Logic Synthesis (IWLS)*, pp. 21–22, 1993.

[29] K. Ho and S. Vrudhula, "A new algorithm for two dimensional multiple folding," in *Proceedings of the ACM/SIGDA Physical Design Workshop*, pp. 117–128, April 1993.

[28] Y.-T. Lai, M. Pedram, and S. Vrudhula, "BDD based logic decomposition with applications to fpga synthesis," in *Proceedings of the IEEE Design Automation Conference (DAC)*, pp. 642–647, June 1993.

[27] A. Majumdar and S. Sastry, "Statistical analysis of controllability," in *Proceedings of the International Conference on VLSI Design*, (Bombay, India), pp. 55–60, January 1993.

[26] A. Majumdar and S. Sastry, "On the distribution of fault coverage and test length in random testing of combinational circuits," in *Proceedings of the IEEE Design Automation Conference (DAC)*, pp. 341–346, June 1992.

[25] Y.-T. Lai and S. Sastry, "Edge-valued binary decision diagrams for multi-level hierarchical verification," in *Proceedings of the IEEE Design Automation Conference (DAC)*, pp. 608–613, June 1992.

[24] Y.-T. Lai, S. Sastry, and M. Pedram, "Boolean matching using binary decision diagrams with applications to logic synthesis and verification," in *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, pp. 452–458, October 1992.

[23] A. Majumdar and S. Sastry, "Distribution and moments of test length," in *Proceedings of the Workshop on New Directions for Testing, Montreal*, (Montreal, Canada), pp. 130–146, May 1992.

[22] Y.-T. Lai and S. Sastry, "An efficient matching algorithm using BDDs for logic verification," in *Proceedings of the 6th Workshop on New Directions for Testing*, (Montreal, Canada), May 1992.

[21] A. Abdullah and S. Sastry, "Topological via minimization and routing," in *Proceedings of the 1st Great Lakes Symp. on VLSI*, pp. 220–224, March 1991.

[20] S. Sastry and A. Majumdar, "A branching process model for observability analysis of combinational circuits," in *Proceedings of the IEEE Design Automation Conference (DAC)*, pp. 452–457, June 1991.

[19] K. Ho and S. Sastry, "Flexible transistor matrix (ftm)," in *Proceedings of the IEEE Design Automation Conference (DAC)*, pp. 475–480, June 1991.

[18] S. Sastry and A. Majumdar, "A stochastic model for fault propagation in combinational circuits," in *Proceedings of the International Symposium on Circuits and Systems (ISCAS)*, pp. 1964–1965, June 1991.

[17] Y.-T. Lai and S. Sastry, "Hints: A hardware interpretation system," in *Proceedings of the International Workshop on Formal Methods VLSI Design*, (Miami, FL), pp. 10–21, January 1991.

[16] S. Sastry and A. Majumdar, "Stochastic models for testing of combinational circuits," in *Proceedings of the 9th Australian Microelectronics Conference*, pp. 19–23, July 1990.

[15] C. Ravikumar and S. Sastry, "Parallel algorithms for coloring perfect graphs with applications to VLSI layout and synthesis," in *Proceedings of the 4th Annual Parallel Processing Symp.*, pp. 587–596, April 1990.

[14] F. Kurdahi and S. Sastry, "Characterization of wire length distributions for standard cell layouts," in *Proceedings of the European Design Automation Conference (EDAC)*, pp. 673–674, March 1990.

[13] C. Ravikumar and S. Sastry, "A parallel algorithm for coloring interval graphs with applications to gate matrix layout and register allocation," in *Proceedings of the International Conference on VLSI*, (Bangalore, India), pp. 189–192, December 1989.

[12] C. Ravikumar and S. Sastry, "A parallel approach to three layer channel routing," in *Proceedings of the International Workshop on Hardware Accelerators for CAD*, (Oxford University, U.K.), pp. 259–272, 1989.

[11] C. Ravikumar and S. Sastry, "LARA : A layout accelerator based on reduced array architecture," in *Proceedings of the International Workshop on Hardware Accelerators for CAD*, (University of Oxford, U.K.), pp. 233–244, 1989.

[10] C. Ravikumar and S. Sastry, "Parallel placement on hypercube architecture," in *Proceedings of the International Conference on Parallel Processing*, pp. 97–101, 1989.

[9] S. Sastry and J. Pi, "An investigation into statistical properties of partitioning and placement problems," in *Proceedings of the IEEE Design Automation Conference (DAC)*, pp. 382–387, June 1989.

[8] C. Ravikumar, S. Sastry, and L. Patnaik, "A data parallel approach to local search placement algorithms," in *Proceedings of the International Conference on VLSI*, (Bangalore, India), pp. 13–20, December 1988.

[7] C. Ravikumar and S. Sastry, "Parallel placement on reduced array architecture," in *Proceedings of the IEEE Design Automation Conference (DAC)*, pp. 121–127, June 1988.

[6] V. P. Kumar and S. Sastry, "A general purpose VLSI array for efficient signal and image processing," in *Proceedings of the International Conference on Parallel Processing*, pp. 917–920, 1987.

[5] S. Sastry and M. Breuer, "Analysis of BIST techniques for CMOS stuck-open faults," in *Proceedings of the International Workshop on Designing for Yield*, (University of Oxford, U.K.), pp. 249–259, July 1987.

[4] S. Sastry and A. Parker, "On the relation between wire length distributions and placement of logic on master slice ICs," in *Proceedings of the IEEE Design Automation Conference (DAC)*, pp. 710–711, June 1984.

[3] S. Sastry and A. Parker, "The complexity of two-dimensional compaction of VLSI layouts," in *Proceedings of the IEEE International Conference on Circuits and Computers*, pp. 402–406, 1982.

[2] S. Sastry and S. Klein, "PLATES: a metric-free VLSI layout language," in *Proceedings of the MIT Conference on Advanced Research in VLSI*, pp. 165–174, January 1982.

[1] S. Klein and S. Sastry, "Parameterized modules and interconnections in unified hardware descriptions," in *Proceedings of the 5th International Conference on Computer Hardware Description Languages and their Applications*, (Kaiserslautern, Germany), pp. 185–195, 1981.

Online Archive

[1] N. Kulkarni and S. Vrudhula, "Efficient enumeration of unidirectional cuts for technology mapping of boolean networks," *arXiv.org*, vol. cs.DS, Mar. 2016. First release date: Sept. 11, 2014.

Awarded

[8] S. Yu, Y. Cao, J. sun Seo, S. Vrudhula, and J. Ye, "A resistive cross-point architecture for robust data representation with arbitrary precision." US Patent 9,466,362, October 2016.

[7] S. Vrudhula and N. Kulkarni, "Robust low power reconfigurable threshold logic array." US Patent 9,490,815, November 2016.

[6] S. Vrudhula and N. Kulkarni, "Spintronic Threshold Logic Gate and Spintronic Threshold Logic Array." US Patent 9,306,151, April 2016.

[5] S. Vrudhula and N. Kulkarni, "Technology mapping for threshold and logic gate hybrid circuits." US Patent 8,832,614, 2014.

[4] S. Vrudhula, S. Bhardwaj, and P. Ghanta, "Method for the analyzing uncertainty in the electrical response characteristics of interconnect wires and general networks of passive electrical components in the presence of manufacturing process variations." US Patent 7,630,852 B1, 2013.

[3] S. Vrudhula and T. Gowda, "A decomposition based approach for the synthesis of threshold logic circuits." US Patent 8,601,417, 2013.

[2] S. Vrudhula and S. Leshner, "A low power, high speed threshold logic element." US Patent 8,164,359, 2012.

[1] S. Vrudhula and T. Gowda, "Combinational equivalence checking for threshold logic circuits." US Patent 8,181,133, 2012.

Pending

[12] "Using Sparse Representation for Weight Memory Compression in Neural Networks." (with Shihui Yin, Jae-sun Seo, Chisung Bae, Sang Joon Kim).

[11] S. Vrudhula, N. Kulkarni, and A. Dengi, "A novel skewed clock generating flipflop (SygnalFF), and a novel clock skewing strategy (SygnalC) to reduce dynamic power and eliminate hold-time violations in synchronos digital VLSI designs." Patent Pending.

[10] S. Vrudhula, J. Davis, N. Kulkarni, and A. Dengi, "A method of obfuscating digital logic circuits using threshold voltage." Patent Pending.

[9] S. Vrudhula and N. Kulkarni, "Threshold Logic Element with Stablizing Feedback, note = Patent Pending."

[8] S. Vrudhula, N. Kulkarni, and J. Yang, "Integration of threshold logic gates with RRAM devices for energy efficient and robust operation." Patent Pending.

[7] S. Vrudhula and N. Kulkarni, "An energy efficient, robust differential mode D-flip-flop (KVFF)." Patent Pending.

[6] S. Vrudhula and V. Hanumaiah, "Performance and energy optimal DVFS, task migrationand active cooling for multi-core processors." Patent Pending.

[5] S. Vrudhula, M. Hamzeh, and A. Shrivastava, "An efficient and register aware compiler technique for mapping applicattions on coarse-grained reconfigurable accelerators." Patent Pending.

[4] "STEAM: A smart temperature and energy aware multicore controller." (with Vinay Hanumaiah, Digant Desai).

[3] "Temperature-aware robust controller for multi-core processors." (with Vinay Hanumaiah, Benjamin Gaudette).

[2] "Parallel architecture with resistive crosspoint array for on-chip learning." (with Yu Cao, Jae-sun Seo, Shimeng Yu).

[1] "Method and apparatus to enhance read accuracy in resistive crosspoint array." (with Yu Cao, Jae-sun Seo, Shimeng Yu).

Period	Title	Source	Share	≈ AMT
2015-2016	NSF Innovation Corps	NSF	100%	$50,000
2015-2017	Scalable and Power-Efficient Compressive Sensing CMOS Image Sensors and Reconstruction Circuits	NSF	50%	$200,000
2014-2016	Testability and Timing Analysis in Nanoscale Designs in the Presence of Process Variations	NSF	50%	$200,000
2014-2015	I/UCRC Center for Embedded Systems	Industry	100%	$300,000
2014-2019	I/UCRC Center for Embedded Systems (Phase II)	NSF	100%	$300,000
2012-2014	Novel Circuit Architectures and Design Methodologies for Low Power Digital Systems	NSF	100%	$600,000
2012-2014	Design of Robust Threshold Logic Circuits	NSF	50%	$200,000
2008-2014	I/UCRC Center for Embedded Systems (Phase I)	NSF, Industry	100%	$1,650,000
2008-2010	A novel threshold logic based circuit architecture for high performance, low power digital circuits	SFAz	100%	$490,000
2008-2011	An Integrated Design Framework for Application Development on Multi-core Processors	SFAz	50%	$2,000,000
2007-2010	Synthesis, Verification and Testing for Nano-CMOS and Beyond using Threshold Logic	NSF	100%	$200,000
2005-2006	I/UCRC Planning Grant for Center for Embedded Systems	NSF	100%	$10,000
2005-2008	Analytical Techniques for Global Energy Minimization of a Systems of Interacting Components	NSF	100%	$450,000
2002-2006	Methodologies for Robust Design of Information Systems under Multiple Sources of Uncertainty	NSF	33%	$2,500,000
1996-2004	Center for Low Power Electronics	NSF, AZ, Industry	100%	$8,000,000
1999-2000	US-Poland Research Collaboration	NSF	100%	$31,000
1999-2000	1999 NSF S/IUCRC Symposium	NSF	100%	$40,000
1998-2000	A Development System for Rapid Prototyping of Dynamically Reconfigurable Mixed-Signal Low-Power Systems	NSF	100%	$250,000
1997-1998	Test Generation using RTL Descriptions	Sunrise Test Systems	100%	$25,000

Period	Title	Source	Share	≈ AMT
1997-1998	Power Models of Cache Memory Subsystem	Motorola Somerset	100%	$44,000
1996-2000	Hardware and Software Co-Design for High Performance Systems	NSF	33%	$563,000
1995-1996	Higher Order Power Models for Estimation and Synthesis for Low Power	Motorola AZ	100%	$64,000
1994-1995	Techniques for CMOS Power Estimation and Synthesis for low power	Motorola AZ	100%	$57,000
1995-1996	Design of an asynchronous, micropiplined floating point unit	IBM Rochester	100%	$40,000
1995-1996	Design of an asynchronous, micropiplined floating point unit	IBM Rochester	100%	$40,000
1993-1994	An Undergraduate Digital Systems Laboratory with Emphasis on VLSI	NSF	100%	$45,000
1993-1994	An Undergraduate VLSI Design Laboratory	Honey-well	100%	$75,000
1993-1994	Stochastic Models in Partitioning for Testability of Digital Circuits	NSF	100%	$60,000
1987-1990	Research in VLSI Design	Powell Founda-tion	100%	$225,000

- *Reducing Power, Leakage and Area using Threshold Logic Gates*, National University of Singapore, Jan. 25, 2014.
- *C-Programmable Coarse-Grain Reconfigurable Hardware Accelerator: Architecture for a Signal Processing Co-Processor*, Raytheon Missle Systems, Tucson, AZ, Feb. 24, 2014.
- *Spintronic Threshold Logic Array (STLA): A Compact, Low Leakage, Non-Volatile Gate Array Architecture*,
  - Everspin Inc., Chandler AZ, Jan. 25, 2013.
  - Qualcomm, Inc. San Diego, CA, Feb. 1, 2013.
- *Reliable Design with Unreliable Components*, NSF/SRC/DFG Joint Workshop on "Bugs and Defects in Electronic Systems: The Next Frontier", April, 22, 2013.
- *Digital Design using Threshold Logic Cells*
  - Texas Instruments Inc., July 15, 2013.
  - Broadcom Inc., Nov. 26, 2013
- *Energy Efficient Computing*, **Keynote Talk** at IEEE International Conference on Computer Systems and Industrial Informatics (ICCSII), Sharjah, United Arab Emirates, Dec. 18-20, 2012.
- *Spintronic Threshold Logic Array (STLA) A Compact, Low Leakage, Non-Volatile Gate Array Architecture*, NANOARCH 2012, Amsterdam, Netherlands, July 5, 2012.
- *Thermal Aware Performance Optimization of Multicore Processors*, Karlsruhe Institute of Technology, Karlsruhe, Germany, July 2, 2012.
- *Digital Design with Threshold Logic*
  1. Karlsruhe Institute of Technology, Karlsruhe, Germany, July 2, 2012.
  2. Qualcomm Inc., San Diego CA, May 31, 2012.
  3. Airforce Research Laboratory, Kirtland Airforce Base, Albuquerque, NM, March 23, 2012.
- *A Balanced 4-Moduli Set and its Reverse Converter Design for Efficient FIR Filter Implementation*, Great Lakes VLSI Symposium, Ecole Polytechnique, Lasusanne Switzerland, April 11, 2011.
- *Boosting Performance per Watt*
  1. Qualcomm Inc., San Diego CA., Sept, 9, 2010.
  2. Granite Ventures Inc., Phoenix AZ, Feb. 12, 2010.
  3. Cypress Semiconductor Inc., San Jose CA, June 4, 2011.
  4. Texas Instruments Inc., Dallas TX, June 6, 2011.

- *Mutlticore Thermal Management*, Intel Inc. Chandler, AZ, Feb 05, 2010.
- *Design space exploration and dyanamic thermal management of multicore processors*,
  1. NSF Workshop on the Science of Power Management, April 9, 2009.
  2. AMD Inc., Santa Clara, CA., Nov 12, 2008.
- *Multicore performance optimization under thermal constraints*, Microsoft Corp., Seattle, WA., May 1, 2008.
- *A unified approach to statistical analysis of full-chip leakage and timing in the presence of process variations*, **invited talk** given at Broadcom Inc., Irvine, CA., Aug. 19, 2008.
- *Performance optimization of multi-core processors under thermal constraints*, **Invited Talk** given at
  1. Seoul National Univeristy, South Korea, Jan. 25, 2007.
  2. Microsoft Inc., Seattle, Washington, Sept. 14, 2007.
  3. Intel Corp., Chandler Arizona, Sept. 20, 2007.
- *Statistical Analysis of Leakage and Timing*, **Keynote Talk** given at 3rd Annual CLEAN (Controlling LEAkage power in NanoCMOS SOC's) Worshop, Gothenburg Sweden, Sept. 6, 2007.
- *Computation of Joint Timing Yield of Sequential Networks considering Process Variations*, International Workshop on Power And Timing Modeling, Optimization and Simulation (PATMOS), Sept. 3, 2007, Goteborg, Sweden.
- *Analysis of Leakage and Timing in the presence of process variations*, LSI Logic Inc., Aug. 30, 2007.
- *Robust design of nano-scale circuits in the presence of process variations*, Full-day tutorial given at the IEEE International Conference on VLSI Design, Bangalore, India, Jan 7, 2007.
- *Stochastic Analysis of interconnects and power grids in the presence of process variations*, First International Workshop on Interconnect Design and Variability, Bangalore, India, Dec. 28-29, 2006.
- 3-Day Tutorial, Texas Instruments, Bangalore, Dec. 19-21, 2006.
  - VLSI Circuit Simulation - Dec. 19, 2006
  - Determinisitic Static Timing Analysis - Dec. 19, 2006
  - Source & Impact of Process Variations - Dec. 20, 2006
  - Statistical Models of Interconnects & Gates - Dec. 20, 2006
  - Statistical Timing & Leakage Analysis - Dec. 21, 2006
  - Optimization in the presence of process variations - Dec. 21, 2006

- *Methodology for the robust design of nano-scale circuits in the presence of process variations*, Freescale Inc., Austin TX, May 17, 2006.
- *Statistical timing and leakage analysis in the presence of process variations*, Freescale Inc., Austin TX, May 17, 2006.
- *Energy Management in Battery Powered Embedded Systems*, EECS Dept., University of Michigan, Ann Arbor, MI Mar. 2004.
- *Analysis and Optimization of Power and Performance of Digital Circuits and Systems*, ST Microelectronics, Phoenix, AZ, Feb. 2004.
- *Statistical Approach to Signal Integrity and Performance Analysis of DSM CMOS Circuits*, Connection One, Arizona State University, Jan. 2004.
- *Battery-Aware Design of Portable Embedded Systems*, **Distinguished Speaker**, Embedded Systems Research Center (ESRC), Seoul National University, Aug. 28, 2003.
- *Identification of the Minimum Leakage States*, Cadence Inc., San Jose CA, Oct. 2003.
- *Statistical Gate Sizing to Improve Timing Yield*
  - Cadence Inc., San Jose CA, Oct. 2003.
  - TAU Workshop, Austin TX, Feb. 2004.
- *Approaches to Minimizing Subthreshold Leakage*, Mindspeed Inc., Irvine CA, June 2003.
- *Energy Management in Battery Powered Embedded Systems*, IBM ARL, Austin, TX, June 2003.
- *Probabilistic Analysis of Interconnect Coupling Noise in Deep Submicron Circuits*
  - **Distinguished Speaker**, Silesian University of Technology, Gliwice, Poland, June 2001.
  - **Distinguished Speaker**, University of Mining and Metallurgy, Akademia Gorniczo-Hutnicza, June 2001.
  - Motorola Inc., Austin TX, Aug. 2001.
  - Center for Low Power Electronics (nationally broadcast), Oct. 2001.
- *Algorithms for Minimizing Standby Power in Dual VT CMOS Circuits*
  - Intel Corp., Santa Clara, CA, Sept. 1999.
  - Intel Corp., Portland Oregon, Sept. 1999.
  - Sun Microsystems, San Jose, CA Aug. 2000.
  - **Distinguished Speaker**, Silesian University of Technology, Gliwice, Poland, June 2000.
  - **Distinguished Speaker**, University of Mining and Metallurgy, Akademia Gorniczo-Hutnicza, June 2000.
  - Center for Low Power Electronics (nationally broadcast), Apr. 2000.

- *Synthesis Algorithms for Low Power Digital Systems*, Cadence Inc., San Jose, CA 1998
- *Dynamically Reconfigurable Architectures: Opportunities and Challenges*, Panel Session (Chair) International Conference on Computer Design (ICCD), Austin, TX, Oct. 1998.
- *Low Power Electronics: Digital Circuits.* **Keynote Speaker** at the Hughes Low Power/Low Voltage Symposium, Newport Beach, CA, Mar. 20, 1997.
- *Rewiring of Combinational and Sequential Logic for Low Power*, Department of Electrical Engineering, University of Michigan, Ann Arbor, Michigan, Sept. 1997.
- *Techniques for Power Reduction in Combinational and Sequential Logic Circuits*, Mentor Graphics, May 1997.
- *Power Optimization of Combinational and Sequential Logic Circuits*, IBM Hopewell Junction, New York, June 1997.
- *Center for Low Power Electronics*, IBM, Hopewell Junction, NY, June 1997.
- *Register Transfer Level Testing using Edge Valued Binary Decision Diagrams*, Viewlogic Inc., Fremont, CA., Oct. 1996.
- *Edge Valued Binary Decision Diagrams*, International Dahsthul Seminar on Computer-Aided Design and Test, Feb. 1995, Dagstuhl, Germany.
- *Edge Valued Binary Decision Diagrams with Applications to Logic Verification, Synthesis, Spectral Transforms, and Combinatorial Optimization*
  - Fujitsu Laboratories of America, San Jose, CA., Apr. 1995,
  - Electrical Engineering Department, University of California Irvine, CA., May 1995.
- *A Fast and Accurate Technique for Estimating Signal Activity in CMOS Logic Circuits*, Motorola Inc., Chandler AZ., Feb. 1995.
- *Asynchronous Systems Design Methodology.* ECE Department, University of Arizona, Tucson, AZ., Feb., 1995.
- *Low Power Design at the Logic, Register-Transfer & Behavior Levels.* Motorola Inc, Chandler, AZ., Apr. 1994.
- *Synthesis of Asynchronous Systems from Data Flow Specifications.* IBM, Austin, TX, Aug. 19, 1993 and at IBM Rochester, Minn., Nov. 1993.
- *Design and Test for VLSI.* Department of Atomic Energy, Minerals Division, Hyderabad, Andhra Pradesh, India, Dec. 1992.
- *Modelling Fault Propagation for Predicting Fault Coverage and Test Length.* Indian Institute of Technology, New Delhi, India, Dec. 1992.
- *Stochastic Models for Testability Analysis of Digital Circuits.* Department of Electrical Engineering, University of Arizona, Apr. 1992.

- *Stochastic Models for Testability Analysis of Digital Circuits.* Department of Electrical Engineering, Iowa State University, Apr. 1992.
- *A Branching Process Model for Fault Propagation in Combinational Circuits.* Pacific Northwest Test Workshop, Seattle, Washington, 1991.
- *Stochastic Models in Testing of Digital Circuits.* MCC, Austin Texas, Sept. 1990.
- *Testability Analysis and Characterization of Digital Circuits.* Department of Electrical Engineering, UC Irvine, Mar. 1990.
- *LARA : A Layout Accelerator Based on the Reduced Array Architecture.* Department of Computer Science and Automation, Indian Institute of Science, Bangalore, India, Aug. 1988.
- *Statistical Properties of Partitioning and Floorplanning Problems.* Department of Computer Science and Automation, Indian Institute of Science, Bangalore, India, Aug. 1988.
- *VLSI Design Automation and Testing Research at USC.* University of Waterloo, Ontario, Canada, Apr. 1987.
- *Minority Fellowship Awards in Science for Undergraduates.* TRW, El Segundo, CA, Oct. 1987.
- *On Mapping Algorithms to Linear and Fault Tolerant Systolic Arrays.* IEEE International Conference On Computer Design, Port Chester, New York, Oct. 1986.
- *Wireability Analysis of Integrated Circuits.* Hewlett Packard Research Labs., Palo Alto, CA, Dec. 1985.
- *A Metric-Free VLSI Layout Language.* IBM General Technology Division, Hopewell Junction, New York, Aug. 1982.

1. Niranjan Kulkarni *Energy-Efficient Digital Circuit Design using Threshold Logic Gates*, Ph.D. Computer Science, 2016.
2. Mahdi Hamzeh *Compiler and Architecture Design for Coarse-Grained Programmable Accelerators*, Ph.D Computer Science, 2015.
3. Digant Desai *Towards Energy Efficient Computing with Linux : Enabling Task Level Power Awareness and Support for Energy Efficient Accelerator*, MS Computer Science, 2013.
4. Vinay Hanumaiah *Unified Framework for Energy-Proportional Computing in Multicore Processors: Novel Algorithms and Practical Implementation*, Ph.D, Electrical Engineering, 2013.
5. Yang Hu, *Testing of threshold logic latch based hybrid circuits*, MS, Electrical Engineering, 2013.
6. Benjamin Gaudette, *Energy Management in Solar Powered Wireless Sensor Networks*, MS Computer Science, 2012.
7. Tejaswi Lingegowda, *Threshold Logic Properties and Methods: Applications to post-CMOS Design Automation and Gene Regulation Modeling*, Ph.D. 2011
8. Samuel Leshner, *Modeling and implementation of threshold logic circuits and architectures'*, Ph.D 2010
9. Gayathri Chalivendra, *A new RNS 4-moduli set for implementation of FIR filters*, MSEE 2011
10. Saurabh Patel, *Improving resilience against differential power analysis with low area and power overhead using threshold logic*, Saurabh Patel, MSEE, 2010
11. Amit Goel, *Characterization of nanoscale digital circuits for statisical timing and signal integrity analysis*, MSEE 2008.
12. Ravishankar Rao, *Fast and accurate techniques for early design space exploration and dynamic thermal management of multi-core processors*, Ph.D. Electrical Engineering, 2008.
13. Sudheendra Kadri, *Performance driven design space exploration in portable devices powered by fuel cell battery hybrid system*, MSEE 2007.
14. Praveen Ghanta, *Stochastic performance modeling and analysis of VLSI circuits in the presence of process variations*, Ph.D. 2007.
15. Sarvesh Bhardwaj, *Novel techniques for analysis and optimization of nano-scale digital circuits in the presence of process variations*, Ph.D. 2006
16. Ravishankar Rao, *Energy Optimal Speed Control for Components of Portable Systems*, MSEE 2004.
17. Sreeja Raj, *Statistical Timing Analysis*, MSEE 2004.
18. Sridhar Dasika, *Energy Management of Sensor Networks*, MSEE 2004.

19. Kaviraj Chopra, *Symbolic Algorithms for Identifying Minimum and Bounded Leakage States*, MSEE 2004.
20. Raghukiran Sreeramaneni, *Energy Profiler for Hardware-Software Codesign*, MSEE 2003.
21. Sarvesh Bhardwaj, *Analysis of Functional and Delay Noise due to Coupling*, MSEE 2003.
22. Daler Rakhmatov, *Energy Optimization for Portable, Battery Powered Systems*, Ph.D. 2002.
23. Haibo Wang, *Field Programmable Analog Array Synthesis*, Ph.D. 2002.
24. Qi Wang, *Logic Synthesis for Low Power*, Ph.D. 1999.
25. Daler Rakhmatov, *Dynamic Scheduling in Runtime Reconfigurable Systems*, MSEE 1998.
26. Yukti Bareja, *RTL Level Power Estimation*, MSEE 1998.
27. Thomas J. Brown, *Algorithms for Clustering of Dataflow Graphs for Implementation on Dynamically Configurable FPGAs*, MSEE 1998.
28. David Rutishauser, *Object Oriented Simulation of a GPS Receiver*, MSEE 1998.
29. Bryce A. Rasmussen, *A Design of a Counterflow Pipeline Processor*, MSEE 1997.
30. Kendel McCarley, *Design of an High Performance Asynchronous Floating Point Unit*, MSEE 1996.
31. Edwin Tsun, *Design of an High Performance Asynchronous RISC Processor*, MSEE 1996.
32. Tzyh-Yung Wuu, *Automatic Synthesis of Asynchronous Systems from Data-Flow Specifications*, Ph.D. 1995.
33. Hong-Yu Xie, *Gate Level Power Estimation*, MSEE 1995.
34. Oliver Harquin, *Asynchronous Discrete Cosine Transform Processor*, MSEE 1995.
35. King C. Ho, *A Graph Theoretic Approach for Two Dimensional Topological Compaction of Regular VLSI Structures*, Ph.D. 1994.
36. Ang Li, *Partitioning for Pseudo Exhaustive Built-In Self-Test*, MSEE 1991.
37. Yung-Te Lai, *Logic Verification and Synthesis using Function Graphs*, Ph.D. 1993.
38. Amitava Majumdar, *Stochastic Models for Testing of Digital Circuits*, Ph.D. 1992.
39. Ravikumar Chennagiri, *Parallel Algorithms and Architectures for Physical Design of VLSI Circuits*, Ph.D. 1991

Arizona State University:

- University Tenure and Promotion Committee, 2016-2019.
- Search Committee for Director of CIDSE, 2016-2017.
- Undergraduate Program Committee for CSE, 2014-2014, 2015-2016, 2016-2017.
- Graduate Program Committee for CENG, 2013-2014, 2014-2015, 2015-2016, 2016-2017.
- Search Committee for Dean of Fulton School of Engineering, 2015-2016.
- Chair, Faculty Recruiting Committee, *Next Generation Computing*, 2012-2013, 2013-2014, 2014-2015.
- Director of Research, Consortium for Embedded Systems, 2005 -
- Chair, Computer Engineering Program Committee, Fulton School of Engineering, 2009-
- Graduate Program Committee, Committee, Computer Science and Engineering, 2008-2010.
- Personnel Committee, Computer Science and Engineering, 2005-2007.
- Chair, Faculty Recruiting Committee, Committee, Computer Science and Engineering, 2005.
- Academic Senate, Arizona State University, 2005-2006.

University of Arizona:

- Promotion & Tenure Committee, Electrical and Computer Engineering Department, 2002-2004.
- Director Summer Internship Program (SPIN) for CLPE, 1996-2004.
- Chair, Faculty Recruiting Committee, Electrical and Computer Engineering Dept., 1997-1998, 2000-2003.
- Computer Engineering Faculty Recruiting Subcommittee, 1993-1994, 1996.
- Undergraduate Curriculum Committee, Electrical and Computer Engineering Dept., 1996-1997.
- Graduate Student Recruiting and Awards Committee, Electrical and Computer Engineering Dept.
- Computer Engineering Curriculum, Electrical and Computer Engineering Dept., 1992-1993, 1996-1997.
- Peer Evaluation Committee, Electrical and Computer Engineering Dept., 1995-1997.
- Chair, Computer Policy Committee, Electrical and Computer Engineering Dept., 1993-1996.
- International Graduate Admissions, Electrical and Computer Engineering Dept., 1994-1996.

Journal Editorships & Program Commitees

- Associate Editor *IEEE Transactions on Multi-Scale Computing Systems (TMSCS), 2015-2016.*
- Associate Editor *IEEE Transactions on Computer-Aided Design* (TCAD), 2006-2013.
- Associate Editor *ACM Transactions on Design Automation of Electronic Systems* (TODAES), 2006-2009.
- Associate Editor *IEEE Transactions on VLSI Systems*, 1996-1998.
- Member of Editorial Board, *Studia Informatica*, Silesian University of Technology Press, Gliwice, Poland, 2001-2002.
- Member of the Board of Directors: Computer Systems Support Solutions, 1998.
- External Reviewer, Computer Engineering Program, Southern Illinois University, Carbondale, 2002.
- Program Committee Member:
  - *Symposium on Biomorphic Circuits & Systems with Threshold Logic*, (BioTL) 2014.
  - *IEEE/ACM International Symposium on Nanoscale Architectures* (NANOARCH), 2014.
  - *IEEE International Symposium on Low Power Electronic Design* (ISLPED), 2014.
  - *IEEE International Conference on Computer Aided Design* (ICCAD), 2014.
  - *IEEE International Conference on Computer Aided Design* (ICCAD), 2013.
  - *IEEE/ACM Design Automation Conference*, 2001-2004, 2014.
  - *IEEE International Conf on Embedded Software and Systems*, China. 2005.
  - *International. Symposium on Quality Electronic Design* (ISQED), 2003-2006.
  - *Mixed Design of Integrated Circuits and Systems*, Poland, 2000-2001.
  - *Southwest Symposium on Mixed-Signal Design*, 1999.
  - *International Conference on Computer Design* (ICCD), 1993-1997.
  - *NSF S/IUCRC Symposium at the University of Oklahoma*, 1997.
- Chair, Vice-Chair, Organizer Positions:
  - *Organizer* of Special Session on “”Toward On-Chip Cortical Computng”, IEEE/ACM Design Automation Conference (DAC), Sanfrancisco, CA, June 2014.
  - *Organizer* of Special Session on “”Neuron Inspired Computing using Nanotechology”, 9th Asia and South Pacific Design Automation Conference (ASP-DAC), Singapore, 2014.
  - *Chair* Technical Program Comittee (RDIC), *International. Symposium on Quality Electronic Design* (ISQED), 2005-2006.

  - *Chair* Technical Program Committee (Power), IEEE/ACM Design Automation Conference, 2005-2006.
  - *Organizer* and *Chair* of Special Session on "Error Tolerant Design", IEEE/ACM Design Automation Conference, 2005.
  - *Session Chair*, Sensor Networks and Communication Systems, International. Symposium on Low Power Electronic Design (ISLPED), Seoul, Korea, 2003.
  - *Chair, National Science Foundation S/IUCRC Symposium*, 1999.
  - *Vice Chair, IFIP Working Group on Hardware/Software co-Design*, 1998.
  - *Track Chair, IEEE International. Conference on Computer Design (ICCD)*, 1998.
  - *Organizer and Session Chair on Dynamically Reconfigurable Architectures*, IEEE International. Conference on Computer Design (ICCD), 1998.
  - *VLSI/VHSIC Session Chair, Phoenix Conference on Computers and Communications*, 1993.
  - General Chairman of *Second International Workshop on The Economics of Design and Test*, 1993.

- Reviewing and Refereeing
  - Invited External Reviewer for the Portuguese National Science Foundation
  - IEEE International Conference on Computer Design
  - IEEE International Conference on Computer-Aided Design
  - IEEE International Conference on Computers and Communications
  - IEEE VLSI Test Symposium
  - IEEE Design Automation Conference
  - Journal of Electronic Testing and Test Applications
  - ACM Transactions on Design Automation
  - IEEE Transactions on VLSI Systems
  - IEEE Transactions on CAD
  - Journal of Integrated Computer-Aided Engineering
  - IEE Proceedings
  - Proposals for the National Science Foundation

- *IEEE Fellow*, for "*contributions to low power and energy-efficient design of digital circuits and systems*", 2016.
- *Best Paper Award:* "*Digital IP Protection Using Threshold Voltage Control*", with Joseph Davis, Niranjan Kulkarni,Jinghua Yang, Aykut Dengi. International Symposium of Quality Electronic Design (ISQED), 2016.
- *Outstanding Researcher:* School of Computing, Informatics and Decision Systems Engineering, ASU, 2010.
- *Best Researcher:* (Senior Faculty), School of Computing, Informatics and Decision Systems Engineering, ASU, 2011.
- *Best Paper Award:* "A methodology for characterization of large macro cells and IP blocks considering process variations", with Amit Goel, Feroze Taraporevala, Praveen Ghanta. International Symposium of Quality Electronic Design (ISQED), 2008.
- *Outstanding Paper Award:* for "Performance Driven Placement and Routing for Field Programmable Analog Arrays", with Haibo Wang and Olek Palusinski. International Conference on Mixed Design of Integrated Circuits and Systems, Zakopane, Poland, 2001.